REMARKS

Applicant respectfully requests reconsideration and allowance of all of the claims of the application.

Claims 6-10 and 45-53 are pending in the application, with claims 6 and 45 being independent. Applicant herein cancels withdrawn claims 1-5 and 11-44. Applicant herein amends claims 6 and 45 for clarification of the subject matter. Support for the claim amendments can be found in the patent application publication at least at paragraphs [0035] and [0054]-[0055]. No new matter has been added.

Formal Request for an Interview

If the Examiner's reply to this communication is anything other than allowance of the pending claims, then Applicant formally requests an interview with the Examiner. Applicant respectfully requests and encourages the Examiner to call Applicant's representative, using the contact information listed at the Conclusion of this document, to resolve any outstanding issues quickly and efficiently over the phone prior to sending any further Office Actions.

Specification Objections

The Specification stands objected to as allegedly having informalities. Applicant amends the specification herein, as shown above, to address the informalities noted in the Office Action. Applicant respectfully requests that the objections be withdrawn.

Drawing Objections

The drawings stand objected to as allegedly failing to comply with 37 C.F.R. 1.84(p)(5) as including reference characters not mentioned in the description.

Corrected drawing sheets in compliance with 37 C.F.R. 1.121(d) are herein submitted, and attached hereto. Applicant respectfully requests that the objections be withdrawn.

Claim Objections

Claims 6 and 45 stand objected to as allegedly having informalities. Specifically, the Office contends there are antecedent issues with the claims. Applicant herein amends claims 6 and 45. Applicant respectfully requests that the objections be withdrawn.

Cited Documents

The following documents have been applied to reject one or more claims of the Application:

- **Leach:** Leach, U.S. Patent No. 6,625,719
- **Meredith:** Meredith, et al., U.S. Patent Application Publication No. 2003/0212671

Claims 6-10 and 45-53 Are Non-Obvious over Leach in view of Meredith

Claims 6-10 and 45-53 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Leach in view of Meredith. Applicant respectfully traverses the rejection.

Independent claim 6, as presently amended, recites in part (amendments underlined):

> - fetch data connected with the instruction, the data comprising at least a first name that is a literalization of a first process and a second name that is a literalization of a second process, the first name and the second name being obtained using the reflective process algebra,...
> - literalize a result of the composing, including saving the result of the composing...
> - an arithmetic and logic unit configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the first name and the second name ...
> - wherein a synchronization of the microprocessor includes a compiler-created explicit synchronization model based on the reflective process algebra.

Applicant respectfully submits that Leach and Meredith, individually or in combination, fail to disclose, teach, or suggest at least these elements of claim 6.

Claim 6 is amended to include new features including a timing and control unit configured to: "fetch data... the data comprising at least a first name that is a literalization of a first process and a second name that is a literalization of a second process, the first name and the second name being obtained using the reflective process algebra," "literalize a result of the composing, including saving the result of the composing," and "an arithmetic and logic unit configured to perform the composing of

the plurality of processes running in parallel, the composing including deliteralizing the first name and the second name, wherein a synchronization of the microprocessor includes a compiler-created explicit synchronization model based on the reflective process algebra." These features are supported by the Application, as originally filed, at least at paragraphs [0035] and [0055]. During the interview, Applicant's representative understood the Examiner to agree that Leach and Meredith lacked at least these features. Applicant thanks the Examiner for this indication. After a review of the documents cited by the Office, Applicant asserts that neither of the cited documents discloses the above new features as presently recited in claim 6. These features have not previously been considered by the Office.

Leach and Meredith do not disclose, teach, or suggest at least these features and elements of claim 6. Thus, claim 6 is patentable over Leach and Meredith. Applicant respectfully asks the Examiner to withdraw the rejection of this claim.

Independent claim 45, as presently amended, recites in part (amendments underlined):

> - at least one microprocessor that includes one or more components that are synchronized based on a program compiler configured to compile a program written in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name:...
>
> - a timing and control unit for retrieving an instruction from a memory, decoding the instruction, fetching data connected with the instruction, and literalizing a result of a composing of a plurality of processes in parallel, including saving the result of the composing, the data including names obtained by literalizing processes in the reflective process algebra...

- an arithmetic and logic unit configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the names obtained by the literalizing process.

Applicant respectfully submits that Leach and Meredith, individually or in combination, fail to disclose, teach, or suggest at least these elements of claim 45.

Claim 45 is amended to include new features including, "at least one microprocessor that includes one or more components that are synchronized based on a program compiler configured to compile a program written in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name," "a timing and control unit for retrieving an instruction from a memory, decoding the instruction, fetching data connected with the instruction, and literalizing a result of a composing of a plurality of processes in parallel, including saving the result of the composing, the data including names obtained by literalizing processes in the reflective process algebra," and "an arithmetic and logic unit configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the names obtained by the literalizing process." These features are supported by the Application, as originally filed, at least at paragraphs [0035] and [0054].

During the interview, Applicant's representative understood the Examiner to agree that Leach and Meredith lacked at least these features. Applicant thanks the Examiner for this indication. After a review of the documents cited by the Office, Applicant asserts that neither of the cited documents discloses the above new features as presently recited in claim 45. These features have not previously been considered

by the Office.

Leach and Meredith do not disclose, teach, or suggest at least these features and elements of claim 45. Thus, claim 45 is patentable over Leach and Meredith. Applicant respectfully asks the Examiner to withdraw the rejection of this claim.

Dependent claims 7-10 are dependent from independent claim 6 and **dependent claims 46-53** are dependent from independent claim 45. Dependent claims 7-10 and 46-53 are allowable by virtue of this dependency, as well as for additional features that each recites.

For example, Leach and Meredith fail to disclose, teach, or suggest, "wherein the components of the at least one microprocessor are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra," as recited in dependent claim 51.

In rejecting claim 51, the Office contends that Meredith (at paragraphs [0030] and [0047]) teaches the features and elements as recited in dependent claim 51. Office action, page 14. Applicant respectfully disagrees.

Meredith discusses the use of a compiler to compile program language 400, a program language that "is a high-order variant of the π-calculus... the language 400 has the ability to programmatically detect 'liveness'... an indication that a process is alive." Meredith, paragraphs [0052] and [0076]. Additionally, Meredith discusses that "[c]ommunication means can provide guaranteed delivery, efficient routing, security, and priority-based messaging," and "communication means can be used to implement solutions for both asynchronous and synchronous scenarios requiring high performance." Meredith, paragraph [0047].

However, Meredith fails to disclose, teach, or suggest "wherein the components of the at least one microprocessor are synchronized by instructions produced by a compiler that compiles a program written in the reflective process algebra," as recited in dependent claim 51.

Accordingly, dependent claim 51 is allowable for at least these additional reasons.

Conclusion

If any issues remain that would prevent allowance of this application, Applicant requests that the Examiner contact the undersigned representative before issuing a subsequent Action.

Respectfully Submitted,

Lee & Hayes, PLLC
Representative for Applicant

/Patrick D. S. Reed/ Dated: August 27, 2010

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